

**ABSTRACT OF THE DISCLOSURE**

[1017] A technique improves the performance of an integrated circuit design by selectively replacing low  $V_t$  transistors with standard  $V_t$  transistors. The selection of gates for replacement may be based on a multi-path timing analysis. If a low  $V_t$  variant of a gate instance increases a path cycle time as compared to a standard  $V_t$  counterpart, the maximum of the path cycle times for all paths that include the low  $V_t$  variant and the maximum of the path cycle time for these paths with a standard  $V_t$  variant are calculated. If the maximum path cycle time for the path including the low  $V_t$  variant is greater than the maximum path cycle time for the path including the standard  $V_t$  variant, then that low  $V_t$  variant is substituted with a standard  $V_t$  variant. Thus, integrated circuit designs prepared in accordance with the invention may exhibit improved cycle times.